WHAT IS CLAIMED IS:

1. A random access memory device including a temperature sensing circuit, the temperature sensing circuit comprising:

a sensing device configured to hold a sensed voltage that varies with changes in temperature at the sensing device;

a first comparator configured to receive the sensed voltage from the sensing device, the first comparator generating a first output signal;

a second comparator configured to receive the sensed voltage from the sensing device, the second comparator generating a second output signal;

a logic circuit configured to receive the first and second output signals;

a first temperature reference circuit having a plurality of first reference voltages;

a second temperature reference circuit having a plurality of second reference voltages;

a first switch circuit coupled between the first temperature reference circuit and the first comparator, the first switch circuit controlled by the logic circuit such that a first reference voltage is applied to the first comparator;

a second switch circuit coupled between the second temperature reference circuit and the second comparator, the second switch circuit controlled by the logic circuit such that a second reference voltage is applied to the second comparator;

a first trimmer coupled to the first temperature reference circuit, the first trimmer being adjustable to adjust the first reference voltage; and

a second trimmer coupled to the second temperature reference circuit, the second trimmer being adjustable to adjust the second reference voltage.

2. The random access memory device of claim 1 wherein the first trimmer is adjustable to correct for input offset voltage in the first comparator and the second trimmer is adjustable to correct for input offset voltage in the first comparator.

3. The random access memory device of claim 1 wherein the first trimmer are resistors that are is adjustable to correct for input offset voltage in the first comparator and the second trimmer are resistors that are is adjustable to correct for input offset voltage in the second comparator.

4. The random access memory device of claim 1 wherein the first and second trimmers are potentiometers that have adjustable resistance.

5. The random access memory device of claim 1 wherein the first and second trimmers are multiple resistors that may be removed and added to the trimmers in order to provide adjustable resistance.

6. A temperature sensing circuit comprising:

a first and a second comparator each configured to receive a sense voltage that is indicative of a sensed temperature;

a first temperature reference circuit having a plurality of first reference voltages coupled to the first comparator such that the plurality of first reference voltages are alternately compared with the sense voltage;

a second temperature reference circuit having a plurality of second reference voltages coupled to the second comparator such that the plurality of second reference voltages are alternately compared with the sense voltage;

a first trimmer coupled to the first temperature reference circuit and a second trimmer coupled to the second temperature reference circuit, the first and second trimmers being independently adjustable to adjust the plurality of first and second reference voltages.

7. The temperature sensing circuit of claim 6 wherein the first trimmer is adjustable to correct for input offset voltage in the first comparator and the second trimmer is adjustable to correct for input offset voltage in the first comparator.

8. The temperature sensing circuit of claim 6 wherein the first and second trimmers are resistors that are is adjustable to correct for input offset voltage in the first comparator and the second trimmer is adjustable to correct for input offset voltage in the first comparator.

9. The temperature sensing circuit of claim 6 wherein the first and second trimmers are potentiometers that have adjustable resistance.

10. The temperature sensing circuit of claim 6 wherein the first and second trimmers are multiple resistors that may be removed and added to the trimmers in order to provide adjustable resistance.

11. The temperature sensing circuit of claim 6 further including a sensing device configured to sense the sensed voltage that varies with changes in temperature at the sensing device.

12. The temperature sensing circuit of claim 6 further including a logic circuit configured to receive a first output signal from the first comparator and a second output signals from the second comparator.

13. The temperature sensing circuit of claim 12 further including a first switch circuit coupled between the first temperature reference circuit and the first comparator and a second switch circuit coupled between the second temperature reference circuit and the second comparator, the first and second switch circuits controlled by the logic circuit such that the plurality of first and second reference voltages are alternately compared with the sense voltage.

14. The temperature sensing circuit of claim 6 configured to be integrated into a random access memory device.

15. A method of decreasing current consumption in a dynamic memory device, the method including the steps of:

providing a semiconductor memory device with a temperature sensing circuit;

periodically refreshing the memory device at a refresh rate;

sensing the temperature of the dynamic memory device with the temperature sensing circuit and producing a corresponding sensed temperature voltage;

providing a first reference voltage;

comparing the sensed temperature voltage with the first reference voltage using a first comparator with a first offset voltage;

providing a second reference voltage;

comparing the sensed temperature voltage with the second reference voltage using a second comparator with a second offset voltage;

determining whether the sensed temperature voltage is within the first and second reference voltages;

adjusting the first reference voltage to balance the first input offset voltage of the first comparator; and

adjusting the second reference voltage to balance the second input offset voltage of the second comparator.

16. The method of claim 15 further including the step of adjusting the refresh rate based on whether sensed temperature voltage is between the first and second reference voltages.

17. The method of claim 15 further including the step of decreasing the refresh rate when the sensed temperature voltage is between the first and second reference voltages.

18. A random access memory device comprising:

a first and a second comparator each configured to receive a sense voltage that is indicative of a sensed temperature;

first means coupled to the first comparator for alternately comparing a plurality of first reference voltages with the sense voltage;

second means coupled to the second comparator for alternately comparing a plurality of first reference voltages with the sense voltage;

third means coupled to the first means for independently adjusting the plurality of first reference voltages; and

fourth means coupled to the second means for independently adjusting the plurality of second reference voltages.

19. The random access memory device of claim 18 wherein the third means are resistors that are adjustable to correct for input offset voltage in the first comparator and the fourth means are resistors that are adjustable to correct for input offset voltage in the second comparator.